

Application No. 10/632,550  
Attorney Docket: CPAC 1017-7 D5CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being sent by facsimile to:  
 Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450  
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Signed: Paula Faulk Hurley  
 Paula Faulk Hurley

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Marcos Karnezos	Attorney Docket No.: CPAC 1017-7 D5
Application No.: 10/632,550	Examiner: Mai-Huong Tran
Filed: 02 August 2003	Group: 2811
Title: Semiconductor Multi-Package Module Including Stacked-Die Package And Having Wire Bond Interconnect Between Stacked Packages	Confirmation No.: 2570
	Customer No. 22470

INFORMATION DISCLOSURE STATEMENT AFTER ALLOWANCE

Commissioner for Patents  
 P.O. Box 1450  
 Alexandria, VA 22313-1450

Sir:

Applicants submit the below-listed documents to be placed in the file:

- Quck et al., U. S. Patent No. 6,492,726 issued 10 December 2002 for "Chip scale packaging with multi-layer flip chip arrangement and ball grid array interconnection".

Respectfully submitted,

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By:

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Date: 17 August 2005

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